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1 Translating between itanium and sparc memory consistency models
Lisa Higham, LillAnne Jackson
July 2006 **SPAA '06:** Proceedings of the eighteenth annual ACM symposiu
algorithms and architectures
Publisher: ACM Request Permissions
Full text available: Pdf (258.74 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 36, Citation

Our general goal is to port programs from one multiprocessor architectu
ensuring that each program's semantics remains unchanged. This paper
problem by determining the relationships between memory consistency

Keywords: itanium, memory consistency models, multiprocessors, pro
sparc

2 Speculation techniques for improving load related instruction schedu
Adi Yoaz, Mattan Erez, Ronny Ronen, Stephan Jourdan
May 1999 **ISCA '99:** Proceedings of the 26th annual international sympos
architecture
Publisher: ACM
Full text available: Publisher Site , Pdf (164.15 KB) Additional Information: full citatio
index terr

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 42, Citation

State of the art microprocessors achieve high performance by executing
cycle. In an out-of-order engine, the instruction scheduler is responsible
instructions to execution units based on dependencies, latencies, ...

Also published in:
May 1999 **SIGARCH Computer Architecture News** Volume 27 Issue 2

3 Feedback-directed memory disambiguation through store distance a
Changpeng Fang, Steve Carr, Soner Önder, Zhenlin Wang
June 2006 **ICS '06:** Proceedings of the 20th annual international conferen
Publisher: ACM Request Permissions
Full text available: Pdf (696.61 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 25, Citation

Feedback-directed optimization has developed into an increasingly impc
optimizing compilers. Based upon profiling, memory distance analysis h
predicting data locality and memory dependences, and has seen ...

Keywords: memory disambiguation, store distance

4 Instruction set synthesis with efficient instruction encoding for configi
Jong-Eun Lee, Kiyoung Choi, Nikil D. Dutt
January 2007 **Transactions on Design Automation of Electronic Systei**
Issue 1
Publisher: ACM Request Permissions
Full text available: Pdf (1.48 MB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 69, Citation

Application-specific instructions can significantly improve the performan
code size of configurable processors. While generating new instructions
operation patterns has been a common way to improve ...

Keywords: Application-specific instruction set processor (ASIP), ISA cu
specialization, bitwidth-economical, configurable processor, instruction e

5 Java consistency: nonoperational characterizations for Java memory
Alex Gontmakher, Assaf Schuster
November 2000 **Transactions on Computer Systems (TOCS)** , Volume 18 I
Publisher: ACM Request Permissions
Full text available: Pdf (305.72 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 29, Citation

The Java Language Specification (JLS) [Gosling et al. 1996] provides an
the consistency of shared variables. The definition remains unchanged i
currently under peer review, which relies on a specific abstract ...

Keywords: Java memory models, multithreading, nonoperational speci

6 Reducing Design Complexity of the Load/Store Queue
Il Park, Chong Liang Ooi, T. N. Vijaykumar
December 2003 **MICRO 36:** Proceedings of the 36th annual IEEE/ACM Intei
Microarchitecture
Publisher: IEEE Computer Society
Full text available: Pdf (174.73 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 42, Citation

With faster CPU clocks and wider pipelines, all relevantmicroarchitecture
accordingly.There have been many proposals for scaling the issue queu
hierarchy. However, nothing has beendone for scaling the ...

7 Fire-and-Forget: Load/Store Scheduling with No Store Queue at All

Samantika Subramaniam, Gabriel H. Loh
December 2006 **MICRO 39:** Proceedings of the 39th Annual IEEE/ACM Inte
Microarchitecture
Publisher: IEEE Computer Society
Full text available: Pdf (357.14 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 32, Citation

Modern processors use CAM-based load and store queues (LQ/SQ) to su
memory scheduling and store-to-load forwarding. However, the LQ and
sizes required for large-window, high- ILP processors. Past research has

8 Co-synthesis of pipelined structures and instruction reordering const
processors
Ing-Jer Huang
January 2001 **Transactions on Design Automation of Electronic Syste**
Issue 1
Publisher: ACM Request Permissions
Full text available: Pdf (1.58 MB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 28, Citation

This paper presents a hardware/software co-synthesis approach to pipe
processor) design. The approach synthesizes the pipeline structure from
architecture (behavioral) specification. In addition, it generates ...

Keywords: compiler instruction optimization\, instruction set processor
taxonomy, synthesis

9 Parallelizing load/stores on dual-bank memory embedded processor
Xiaotong Zhuang, Santosh Pande
August 2006 **Transactions on Embedded Computing Systems (TECS)** ,
Publisher: ACM Request Permissions
Full text available: Pdf (746.64 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 57, Citation

Many modern embedded processors such as DSPs support partitioned n
X--Y memory or dual-bank memory) along with parallel load/store instr
code density and performance. In order to effectively utilize the ...

Keywords: DSP architectures, memory bank allocation, parallel load/st
optimization

10 Link-time compaction and optimization of ARM executables
Bjorn De Sutter, Ludo Van Put, Dominique Chanet, Bruno De Bus, Koen De
February 2007 **Transactions on Embedded Computing Systems (TECS)**
Publisher: ACM Request Permissions
Full text available: Pdf (636.53 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 112, Citatio

The overhead in terms of code size, power consumption, and execution
precompiled libraries and separate compilation is often unacceptable in
where real-time constraints, battery life-time, and production ...

Keywords: Performance, compaction, linker, optimization

11 Assembly instruction level reverse execution for debugging
Tankut Akgul, Vincent J. Mooney III
April 2004 **Transactions on Software Engineering and Methodology (**
Publisher: ACM Request Permissions
Full text available: Pdf (1.18 MB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 27, Downloads (12 Months): 72, Citatior

Assembly instruction level reverse execution provides a programmer wi
program to a previous state in its execution history via execution of a "r
ability to execute a program in reverse is advantageous for ...

Keywords: Debugging, reverse code generation, reverse execution

12 On the value locality of store instructions
Kevin M. Lepak, Mikko H. Lipasti
June 2000 **ISCA '00:** Proceedings of the 27th annual international sympos
architecture
Publisher: ACM
Full text available: Pdf (149.50 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 33, Citation

Value locality, a recently discovered program attribute that describes th
recurrence of previously-seen program values, has been studied enthus
published literature. Much of the energy has focused on refining ...

Also published in:
May 2000 **SIGARCH Computer Architecture News** Volume 28 Issue 2

13 Toward kilo-instruction processors
Adrián Cristal, Oliverio J. Santana, Mateo Valero, José F. Martínez
December 2004 **Transactions on Architecture and Code Optimization (**
Publisher: ACM Request Permissions
Full text available: Pdf (1.16 MB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 61, Citation

The continuously increasing gap between processor and memory speed:
the performance achievable by future microprocessors. Currently, proce
memory operations largely by maintaining a high number of ...

Keywords: Memory wall, instruction-level parallelism, kilo-instruction p
multicheckpointing

14

An efficient single-pass trace compression technique utilizing instruc
Aleksandar Milenković, Milena Milenković
January 2007 **Transactions on Modeling and Computer Simulation (TC**
Publisher: ACM Request Permissions
Full text available: Pdf (848.21 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 44, Citation

Trace-driven simulations have been widely used in computer architectui
evaluations of new ideas and design prototypes. Efficient trace compres
decompression are crucial for contemporary workloads, as representati\

Keywords: Instruction and data traces, instruction streams, trace com

15 The KScalar simulator
J. C. Moure, Dolores I. Rexachs, Emilio Luque
March 2002 **Journal on Educational Resources in Computing (JERIC)**
Publisher: ACM Request Permissions
Full text available: Pdf (493.35 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 80, Citatior

Modern processors increase their performance with complex microarchit
makes them more and more difficult to understand and evaluate. KScal
tool that facilitates the study of such processors. It allows ...

Keywords: Education, pipelined processor simulator

16 GPGPU: general purpose computation on graphics hardware
David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ia
Aaron Lefohn
August 2004 **SIGGRAPH '04:** SIGGRAPH 2004 Course Notes
Publisher: ACM Request Permissions
Full text available: Pdf (63.03 MB) Additional Information: full citation, abstract, cit

Bibliometrics: Downloads (6 Weeks): 125, Downloads (12 Months): 1421, Cit

The graphics processor (GPU) on today's commodity video cards has ev
powerful and flexible processor. The latest graphics architectures provid
bandwidth and computational horsepower, with fully programmable ver

17 Adapting compilation techniques to enhance the packing of instructic
Stephen Hines, David Whalley, Gary Tyson
October 2006 **CASES '06:** Proceedings of the 2006 international conference
and synthesis for embedded systems
Publisher: ACM
Full text available: Pdf (598.56 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 26, Citation

The architectural design of embedded systems is becoming increasingly
varying constraints regarding energy consumption, code size, and execu

compiler optimizations are often tuned for improving general architectu

Keywords: compiler optimizations, instruction packing, instruction regi

18 Block-aware instruction set architecture
Ahmad Zmily, Christos Kozyrakis
September 2006 **Transactions on Architecture and Code Optimization**
Publisher: ACM Request Permissions
Full text available: Pdf (539.64 KB) Additional Information: full citation, abstract, ref

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 91, Citation

Instruction delivery is a critical component for wide-issue, high-frequen bandwidth and accuracy place an upper limit on performance. The proc and bandwidth are limited by instruction-cache misses, multicycle ...

Keywords: Instruction set architecture, basic block, branch prediction, instruction fetch, software hints

19 Compiler techniques for code compaction
Saumya K. Debray, William Evans, Robert Muth, Bjorn De Sutter
March 2000 **Transactions on Programming Languages and Systems (**
Publisher: ACM Request Permissions
Full text available: Pdf (409.20 KB) Additional Information: full citation, abstract, ref review

Bibliometrics: Downloads (6 Weeks): 15, Downloads (12 Months): 132, Citati

In recent years there has been an increasing trend toward the incorpor variety of devices where the amount of memory available is limited. Thi to reduce the size of applications where possible. This ...

Keywords: code compaction, code compression, code size reduction

20 Commit-reconcile & fences (CRF): a new memory model for architec
Xiaowei Shen, Arvind, Larry Rudolph
May 1999 **ISCA '99:** Proceedings of the 26th annual international sympos architecture
Publisher: ACM
Full text available: Publisher Site , Pdf (154.10 KB) Additional Information: full citatio index ter

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 30, Citation

We present a new mechanism-oriented memory model called Commit-R (CRF) and define it using algebraic rules. Many existing memory models restricted versions of CRF. The model has been designed so that it is ...

Also published in:
May 1999 **SIGARCH Computer Architecture News** Volume 27 Issue 2

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